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Meta-Study on Integrated Cooling of Modern Integrated Circuits using Microfluidics

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Abstract: The substantial increase in the transistor density of integrated circuits (ICs) in recent times has allowed considerable improvements in computing power. With increasing transistor and power density, the heat produced by modern ICs has increased significantly. This in turn has negative effects on the performance, reliability, and power consumption of the ICs. A solution to the IC's complications caused by overheating is integrated cooling, in which cooling fluid is delivered through microchannel heat sinks on the backside of an IC. This meta-study will investigate two microfluidic cooling technologies. First, implementing varied size microfluidic channels close to the silicone substrate of the IC. Additionally, a micro-pin fin heat sink is integrated into the ICs' fluidic microchannels. Different sized pin fins were used, to achieve a wider understanding of the application of pin fins in microfluidic cooling and compare the thermal performances of each cooling method. Integrated cooling subverts the need for suboptimal thermal interfaces and bulky heat-sinks, as well as reducing the intensity of localised hotspots commonly present in high-power electronics. Further, by locating the main heat exchange medium closer to the die of an IC, we reduce the number of thermal interfaces. This meta-study suggests that cylindrical micro-pin fin arrays with pitch longitude and latitude of 60μm and 120μm, are more thermally efficient than plain microfluidic cooling channels.

Keywords: integrated circuits (ICs); microfluidics; tier; cooling; microfluidic cooling; heat hotpots; heat sinks; 3D IC.

Nomenclature

$R_{th}\left(\frac{cm^2K}{W}\right)$: Thermal Resistance per unit area (cm_2K/W)
$R_{th}\left(\frac{K}{W}\right)$: Thermpenal Resistance (K/W)
$P_{Dissipated}$: Heat flux (W/cm_2)
T_{Inlet}: Temperature of inlet fluid (K)
$T_{Junction}$: Temperature at junction of the transistor (K)
ΔT: Temperature difference (in Kelvin) between transistor junction and inlet fluid
α: Aspect ratio height-to-width of a microchannel
H_c: Height of microchannel (in micrometres)
W_c: Width of microchannel (in micrometres)
W_{pp}: Pump power (W)
Q_v: Volumetric flow rate (m_3/s)
ΔP: Pressure drop (Pa)
N: Number of microchannels
Ac: Cross-sectional area of microchannel (cm_2)
v_c: velocity of fluid at inlet of microchannel
e: thermal efficiency index

1. Introduction

In modern computers, compact processing density increases the power density within an advanced computer [1,2]. This increase in power density results in overheating, causing both a decrease in computational power and eventually a breakdown in processor function [2,3]. In traditional forms of cooling, such as direct mounted aluminum heat sinks, or water cooling, the interface between the cooler and the processor is relatively large in comparison to the nano-sized processors. These large interfaces and their design cause inefficiency in cooling, producing hotspots within the chip. This, as well as the physical profile of cooling technologies, limits the accessibility to more powerful and miniaturized devices in the future [1].

1.1 Integrated Cooling

A common approach taken for cooling modern ICs, is microfluidic cooling. Microfluidic cooling was first introduced in 1981 by Tuckerman et al. [4], in an attempt to improve the cooling of very large-scale circuits (VLSCs). In the article, water was used as the coolant for the heat sinks of VLSCs and thus improved the performance of the circuits. In a more recent study Zhang et al., used a microfluidic heat sink (MFHS) to demonstrate the cooling of a 2-tier stack [5,16]. It was found that utilising a MFHS maintained the stack temperature below 50°C for a total power density of 200 W/cm2 in a two-tier stack, preventing the 3D IC from overheating.

Embedded cooling is divided here into three general implementations, as described by Sarvey et al [6,14]. First, integration of microfluidics into a silicon interposer, wherein multiple dice may be mounted. This places the microfluidic heat sink much closer to the heat sources than in a conventional thermal management system. No modification to the original die is required. The second implementation makes use of microfluidic channels integrated into the backside of each die. This can result in better performance as the heat sink is located closer to the heat source, minimizing junction-to-ambient thermal resistance [6,8]. Monolithically integrating microchannels into the die like this can maintain lower junction temperatures [6]. The final implementation, the integration of microfluidic heat sinks in a 3D stack [6,9]. Separate heat sinks are integrated into each high-power tier, on the backside of the die. The benefit of this configuration is flowrates to each tier

can be managed depending on the heat flux of each tier at any moment in time. Tier specific cooling has been shown to reduce pumping power by 37.5% by preventing tiers from being overcooled when low heat flux is present [7].

1.2 Thermal Resistance

While investigating new methods of IC cooling, the performance of two microfluidic cooling technologies were analysed and compared. First the application of different sized microfluidic channels within an integrated circuit and then the integration of pin-fins within the microfluidic channels with varied pitch and aspect ratios. Measuring the thermal resistance (cm^2K/W) within each cooling method is crucial, as it will assist in determining which cooling method performs best [10]. A high thermal resistance indicates that the IC insulates a great amount of heat, causing the IC to overheat and perform poorly. Ideally, a well-functioning integrated cooling mechanism will obtain low thermal resistance as it conducts heat away from the IC.

1.3 Micro-pin fins

Pin-fins were first introduced by Tuckerman et al. in 1984 [11] while investigating efficient cooling methods for ICs. Micro-pin fins allow greater surface area interaction between the heatsink and the fluid. It was found that arrangements of micro-pin fins typically dissipated heat more efficiently and evenly than microchannels [11]. Due to improved mechanical processes cylindrical micro-pin fins are now being investigated and are included in this meta-analysis [12].

1.4 Aim and Objective

This meta-study will focus on two microfluidic cooling technologies. The first is a plain microfluidic cooling channel with varied width and height values. The second includes three different micro-pin fin arrays which vary is dimensions such as pitch longitude and latitude. The aim of this study is to collect and analyse data from various research papers which include these technologies, in order to identify the one which is more thermally efficient.

2. Methods

A thorough research and investigation was conducted for this meta-study. The literature was attained through a number of scientific databases including Scopus, IEEE Xplore, Web of Science and Arxiv. The searches within the databases were restricted to the past 10 years, to ensure the use of the most recent technologies from the extracted information. Additionally, specific keywords were used during the research so that the information found would be as relevant to the meta-study as possible. These keywords include integrated cooling, microfluidic cooling, heat sinks, integrated circuits (ICs) and 3D ICs.

The sources which were analysed for this study were a wide range journals, articles and books specifically focusing on integrated cooling of ICs. In this sense, the extracted data could be used to conclude which cooling method performs best and is more thermally efficient.

2.1 Normalisation of Data

To compare the effectiveness of embedded cooling configurations, it is convenient to normalise a performance metric. Normalising the temperature difference ($T_{Junction}$-T_{Inlet}) between the transistor junction, and the inlet fluid by dividing by the heat flux per area (W/cm^2). This gives the thermal resistance of the cooling package per unit area, R_{th} (cm^{2}K/W) [13].

$$R_{th}\left(\frac{cm^2K}{W}\right) = \frac{T_{Junction} - T_{Inlet}}{P_{Dissipated}} \quad (1)$$

Where $P_{Dissipated}$ is the heat flux per area. A high thermal resistance would be indicative of low heat flux, across a given temperature differential. In the context of IC cooling, lower thermal resistances are better, as the power dissipated by the cooler would be greater for the same ΔT.

3. Results and Discussion

3.1 Effect of Microchannel Size on Thermal Performance

The inclusion of micro-pins, or some other surface area enhancement structure may not be suitable for some applications. Here the effect that aspect ratio has on the thermal performance of plain microchannels is shown [14]. The aspect ratio is defined as the ratio of height to width, per microchannel.

$$\alpha = \frac{H_c}{W_c} \quad (2)$$

Pump power is also of interest when considering cooling of micro-electrics. Minimising the required pumping power reduces the impact of the pump and fluid connections on system packaging. Pump power is defined as:

$$W_{pp} = Q_v \cdot \Delta P \quad (3)$$

where Q_v is the volumetric flow rate and ΔP is the pressure drop across the whole heat sink.

Alternatively, the power is expressed in terms of individual channels, where:

$$W_{pp} = \Delta P \cdot \mathrm{N} \cdot A_c \cdot v_c \quad (4)$$

In the case of N microchannels, of cross-sectional area Ac, and fluid inlet velocity v_c, ΔP is the pressure drop across an individual microchannel. These definitions neglect frictional losses within connecting pipes.

To investigate the relationship between thermal resistance and pumping power, Wang. H et al. [14], compared rectangular microchannels of 12 aspect ratios [14]. All microchannels are of constant cross-sectional area. The variation of area normalised thermal resistance, as a function of pump power is shown in Figure 1.

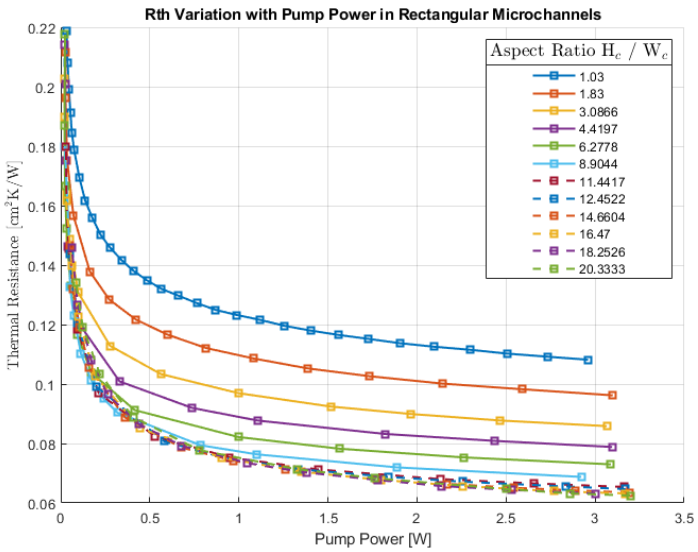

Figure 1. Thermal Resistance varying with Pump Power of rectangular microchannels with different aspect ratios [14].

Increasing the aspect ratio has a generally positive effect for $1 < \alpha < 10$. Beyond an aspect ratio of 10, the reduction in thermal resistance diminishes, thus there is negligible benefit in increasing further. Figure 2 shows the variation of pump power with aspect ratio, while the thermal resistance is kept constant. Initially there is a large decrease in required power as the aspect ratio increases from approximately unity to 5-10. For thermal resistances >0.09, pump power has a minimum for values of α between 6 and 10. Beyond this, there is an upward trend in power, as α increases further. The power increase is attributed to increased frictional losses, as the cross section becomes more eccentric [16].

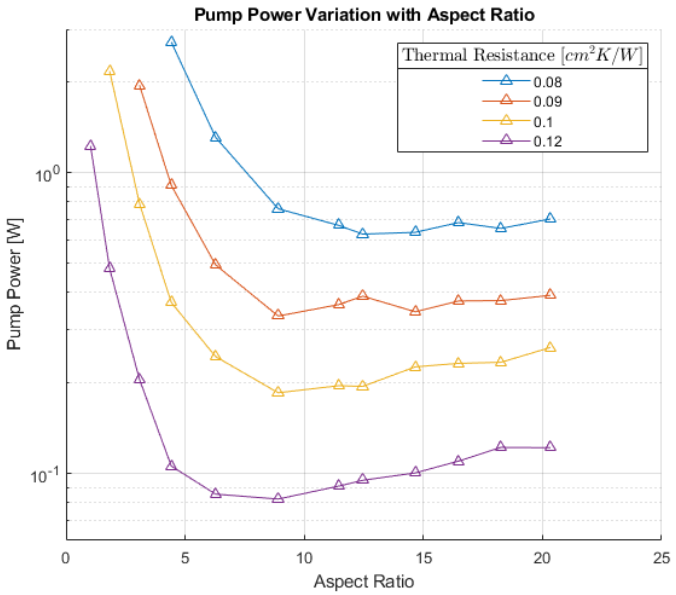

Figure 2. Pump Power varying with Aspect Ratio at thermal resistances of 0.08, 0.09, 0.1 and 0.12 [14].

A similar, more extreme result was investigated by Gonzalez-Hernandez [16], where the overall trends of varying aspect ratios were considered. For three fixed microchannel widths, the channel height was varied. The configurations are as such in Table 1.

Width Level	W_c $[\mu m]$	Height Level	H_c $[\mu m]$
1	147.5	1	25
2	395	2	50
3	890	3	100
		4	200
		5	400
		6	700
		7	1000

Table 1. Microchannel aspect ratio configurations. For each width level, the height level will be altered from 25µm to 1000µm [14-16].

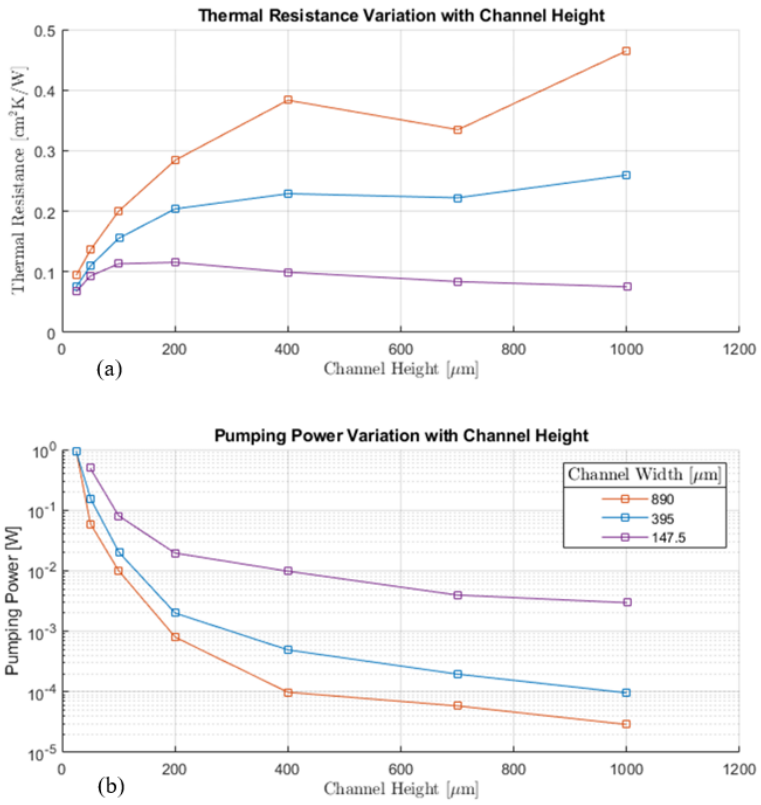

Figure 3. Graph (a): variation of thermal resistance with the channel height at widths of 147.5µm, 395µm and 890µm. Graph (b): pumping power variation with the channel height at widths of 147.5µm, 395µm and 890µm [16].

In all cases, the volumetric flow rate was kept constant. Gonzalez [16] analyses microchannel heatsinks which have aspect ratios of less 1. Consistent with the results of Wang et al. [15] above, the

second graph of Figure 3 shows the variation in pumping power with constant height microchannels. The dramatic increase in pump power for very small aspect ratios is the result of the extreme velocities in the microchannels, causing large friction loses. Figure 3a shows the thermal resistance as channel height increases, for several fixed widths. Thermal resistances below 0.1 cm2K/W are obtained for all channel widths with small channel heights (25-50μm). However, the extreme power required to achieve this thermal resistance precludes the use of such low aspect ratios. Alternatively, a channel width of 147μm, also achieves thermal resistance less than 0.1 cm2K/W when the channel height is greater than approximately 400µm, while also reducing the power required by three orders of magnitude.

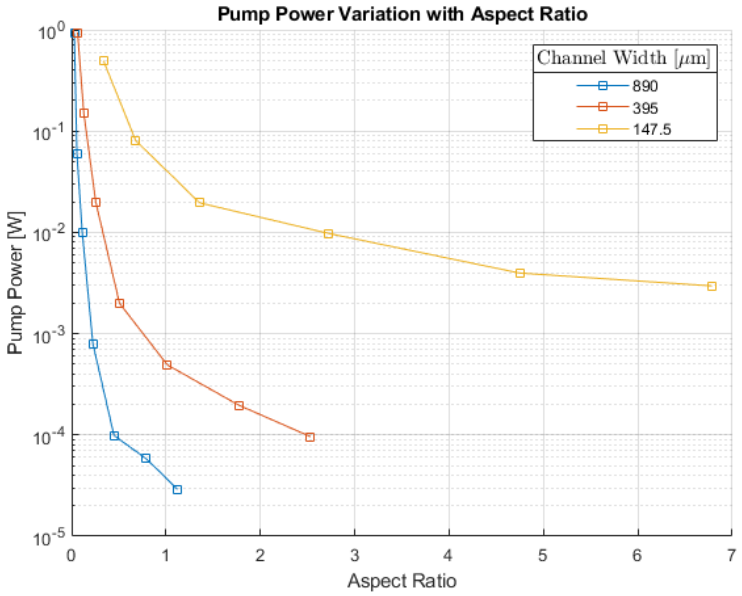

Figure 4. Pump power varying with aspect ratio at widths of 147.5µm, 395µm and 890µm [16].

From the data collected by Gonzalez [16], the trend of pump power variation with aspect ratio is examined. Figure 5 shows the extreme effect that aspect ratios approaching zero have on the power required. Is it clear that in order to examine microchannel performance further, the thermal efficiency index is expressed as:

$$e = \frac{1}{R_{th} \cdot W_{pp}} \tag{5}$$

For an ideal engineering application, both thermal resistance and pumping power must be at a minimum. Thus, the maximum thermal performance is gained, for the minimum input work. A large efficiency index indicates a good work to thermal performance ratio, and vice versa. Figure 5 shows how this metric varies with aspect ratio, at several values of pump power, data obtained from experiments by Wang et al. [15]. To keep pump power constant, linear interpolation of the data was used. A negligible reduction is seen on performance for aspect ratios greater than 10, as suggested earlier. While there seems to be little thermal detriment in increasing the aspect ratio up to 20, there are electrical concerns. Microfluidic cooling improves the feasibility of creating 3D stacked IC architectures. 3D IC's increase the heat flux per unit area, thus making traditional top/bottom heat

sinks comparatively ineffective. Integrating interlayer microfluidic heat sinks could help to improve cooling performance, however TSV's must pass through the heatsink, so minimising height is necessary to reduce undesired TSV capacitance [16]. Therefore, microchannel aspect ratio and height must be optimised to manage trade-offs.

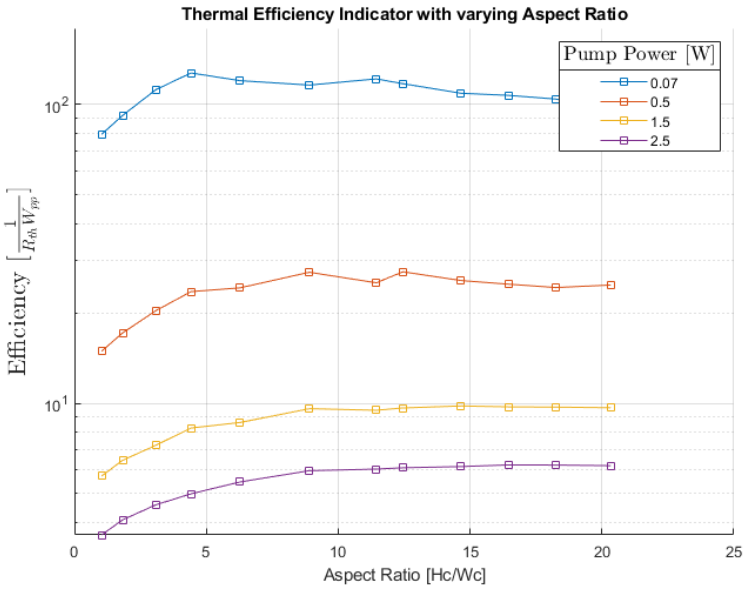

Figure 5. Thermal efficiency index (e) changing with aspect ratio at pump powers of 0.07W, 0.5W, 1.5W and 2.5W [14-16].

As the pumping power decreases, the efficiency index improves markedly. This can be attributed to the increased pressure drop and the rapid decrease in thermal resistance for low pump powers less than 0.2 W. Figure 4 shows that the highest efficiency is attained at a pump power of 0.07W. The aspect ratio is just less than 5 when the efficiency reaches its peak, at approximately 105.

3.2.1 Micro-pin fin geometry

Micro-pin fins integrated into microfluidic cooling systems of ICs vary in size and shape. Micro-pin fin geometries include diamond-shaped, rectangular, circular, triangular, cone-shaped and square [17]. In this meta-study however, circular pin fins with varied dimensions will be used. Based on an experimental study [18] in the International Journal of Heat and Mass Transfer, circular pin fins exbibit a high heat transfer as well as low thermal resistance values. Figure 6 is an illustration of the cross-sectional view of 5 circular micro-pin fins.

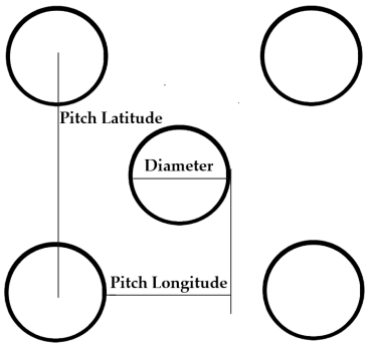

Figure 6. Cross-section of pin fins. Illustration depicts how the dimensions of a micro-pin fin are measured.

3.2.2 Thermal and mechanical effects of pin fin characteristics

The thermal performance of microfluidic cooling devices can be improved by the inclusion of surface area enhancements, including pin fins of various cross sections or dimensions [3,6]. In order to determine the optimal pin fin form factor, data from several sources have been collated. Various micro pin fin cross sections, pitch, and size have been studied in the literature, both in experimental setups and in simulation.

Name	Diameter [µm]	Pitch Long [µm]	Pitch Lat [µm]	Height [µm]
Die 1	30	30	90	202.1
Die 2	30	36	75	196.4
Die 3	30	60	120	197.1

Table 2. Micro-pin fin diameter, pitch longitude, latitude, and height. All measurements are in micrometres [6].

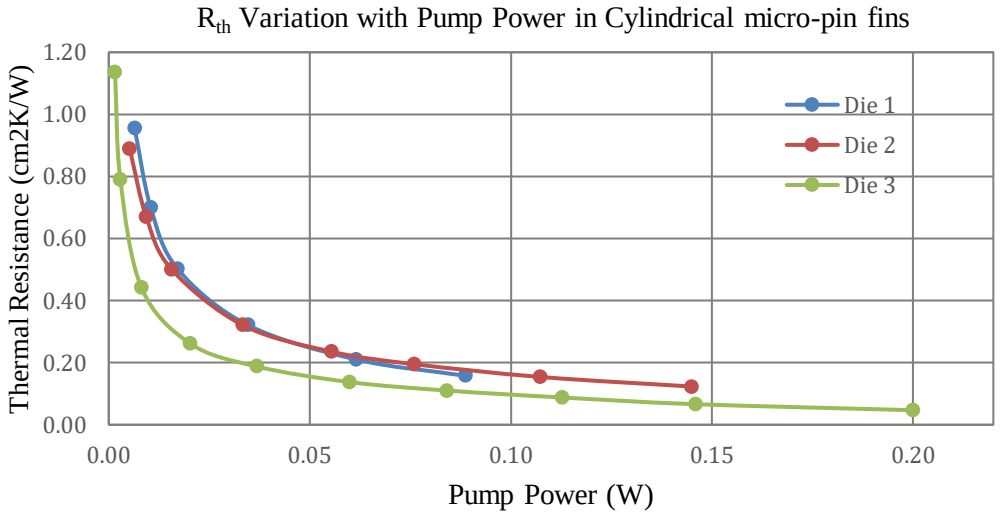

Figure 7. Thermal Resistance varying with Pump Power for the three dice [6].

In this experiment, 3 micro-pin fins with different dimensions have been used. The dimensions (in micrometres) of a pin fin as shown in Table 1 and Figure 6, include the diameter, the pitch longitude and latitude and height.

$$R_{th}\left(\frac{cm^2K}{W}\right) = R_{th}\left(\frac{K}{W}\right) \cdot Chip\ Area\ (cm^2) \qquad (6)$$

The R_{th} (K/W) was given (6), however the thermal resistance per unit area was needed for the comparison between the 3 dice as shown in Figure 7. The R_{th} per unit area was calculated using Eq.

6, where the area of the chip was 1cm2. Having the new R_{th} values for each die, Figure 7 depicts the change in thermal resistance R_{th} of each die with an increasing pump power of the fluid.

The pump power W_{pp} was calculated using Eq. 3 in which the flow rate is multiplied by the pressure drop. Die 1 and 2, possess a similar R_{th} value with an increasing pump power. However, die 3 shows lower thermal resistance. At a pump power of 0.050W, die 1 and 2 have an $R_{th} \approx 0.16$ cm^2K/W, while die 3 has $R_{th} \approx 0.26$ cm^2K/W. Therefore, die 3 has approximately a 38.5% lower thermal resistance than of die 1 and 2.

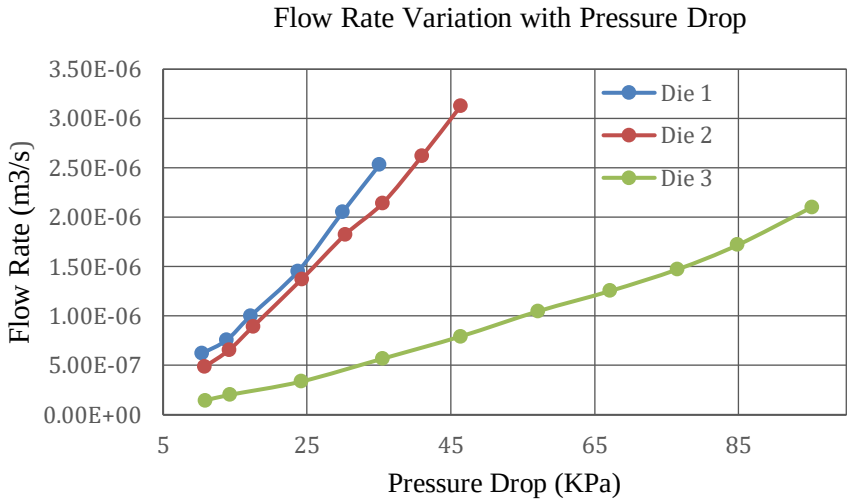

Figure 8. Flow rate of fluid varying with the pressure drop of the microfluidic channel of the three different dice [6].

The graph in Figure 8, depicts the flow rate of the fluid in m3/s changing with pressure drop. Pressure drop refers to the pressure difference between the fluid inlet and outlet of the cooling microchannels. As shown, die 3 has a higher pressure drop than of die 1 and 2. A larger pressure drop in die 3 is expected, since the micro-pin fins have higher pitch longitude and latitude and the volume of the microchannel is greater than of die 1 and 3.

A further examination of microchannel's performance will be expressed by the thermal efficiency index (Eq. 5). The Die 1, 2 and 3 have an efficiency index of 109.2, 107.3 and 215.7 respectively. Across all 3 micro-pin fin arrays with an average height of 198.5±5μm, die 3 is approximately twice as efficient as die 1 and 2. Based on calculations, die 3 reaches a thermal efficiency of 564.7, at a pump power of 1.56×10^{-3}W.

4. Conclusion

This meta-study aimed to investigate the thermal performance and efficiency of two different embedded cooling configurations, with varying dimensional parameters. First, the effect of microchannel aspect ratio on the heat transfer and pumping power. Second, the impact of integrating surface-area enhancements, in this case, micro-pins to the heat sink. Micro-pin diameter, lateral

spacing and longitudinal spacing were varied. An attempt was made to identify optimal parameters for each case.

Thermal performance was evaluated by comparison of thermal resistance values, for each configuration. A lower thermal resistance indicates greater heat transfer for a given temperature difference, indicating greater performance. The efficiency of each channel layout was also compared via pumping power. The data obtained from the thermal measurements of each method was normalized by chip area. For plain microchannels, the thermal resistance decreases with increasing aspect ratio (H/W) between 1.03 and 11.4. Beyond an aspect ratio of 11.4, the thermal performance gain is negligible. For aspect ratios less than 1, the pumping power increases dramatically, making such configurations inefficient. The highest thermal efficiency was achieved by the microchannel with an aspect ratio of ≈ 5 at a pumping power of 0.07W. The thermal efficiency index for that microchannel was ≈105.

On the other hand, the integration of circular micro-pin fin arrays exhibited a better thermal performance. Overall, the thermal efficiency index for die 3 with longitudinal pitch of 60μm and lateral pitch of 120μm was 215.7. That surpasses the efficiency of die 1 and die 2 with efficiencies of 109.2 and 107.3 respectively. Therefore, the cylindrical micro-pin fin array of die 3 has a thermal efficiency greater than twice as that of the plain microchannel.

Although larger microchannel aspect ratios resulted in better thermal characteristics, it should be noted that increasing the total height of the heatsink has a negative effect of through silicon via (TSV) performance [19].

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